

**AMENDMENT TO THE CLAIMS**

This listing of claims replaces all prior listing of claims for the present application.

Claims 1-31 (canceled).

32. (currently amended) A method of forming a capacitor in a semiconductor device, said method comprising:

forming a bottom conducting layer, wherein said bottom conducting layer forms a bottom electrode;

forming a dielectric layer over the bottom conducting layer;

forming a top conducting layer over the dielectric layer, wherein said top conducting layer forms a top electrode; and

annealing ~~the entire~~ a top conducting layer of the top electrode with an oxidizing gas anneal.

33. (original) A method of forming a capacitor of claim 32, wherein said capacitor is formed over a conductive plug, said method further comprising depositing an oxygen barrier over said conductive plug prior to forming the bottom conducting layer.

34. (original) A method of forming a capacitor of claim 32, said method further comprising: annealing the dielectric layer after it is formed.

35. (original) A method of forming a capacitor of claim 32, wherein said bottom conducting layer is formed of a material selected from the noble metal group.

36. (original) A method of forming a capacitor of claim 32, wherein said bottom conducting layer is formed of a metal.

37. (original) A method of forming a capacitor of claim 32, wherein said bottom conducting layer is formed of a metal alloy.

38. (original) A method of forming a capacitor of claim 32, wherein said bottom conducting layer is formed of a conducting metal oxide.

39. (original) A method of forming a capacitor of claim 32, wherein said bottom conducting layer is formed of a metal nitride.

40. (original) A method of forming a capacitor of claim 32, wherein said bottom conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), Platinum Iridium (PtIr), Ruthenium, Ruthenium Oxide ( $\text{RuO}_2$ ), Rhodium Oxide ( $\text{RhO}_2$ ), Chromium Oxide ( $\text{CrO}_2$ ), Molybdenum Oxide ( $\text{MoO}_2$ ), Rhemium Oxide ( $\text{ReO}_3$ ), Iridium Oxide ( $\text{IrO}_2$ ), Titanium Oxides ( $\text{TiO}_1$  or  $\text{TiO}_2$ ), Vanadium Oxides ( $\text{VO}_1$  or  $\text{VO}_2$ ), Niobium Oxides ( $\text{NbO}_1$  or  $\text{NbO}_2$ ), and Tungsten Nitride ( $\text{WN}_x$ ,  $\text{WN}$  or  $\text{W}_2\text{N}$ ).

41. (original) A method of forming a capacitor of claim 40, wherein said bottom conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), Platinum Iridium (PtIr), and Tungsten Nitride (WN<sub>x</sub>, WN or W<sub>2</sub>N).

42. (original) A method of forming a capacitor of claim 32, wherein said dielectric layer is a dielectric metal oxide layer.

43. (original) A method of forming a capacitor of claim 32, wherein said dielectric layer has a dielectric constant between 7 and 300.

44. (original) A method of forming a capacitor of claim 32, wherein said dielectric layer is formed of a material selected from the group consisting of: Tantalum Oxide, Tantalum Pentoxide (Ta<sub>2</sub>O<sub>5</sub>), Barium Strontium Titanate (BST), Aluminum Oxide (Al<sub>2</sub>O<sub>3</sub>), Zirconium Oxide (ZrO<sub>2</sub>), Praseodymium Oxide (PrO<sub>2</sub>), Tungsten Oxide (WO<sub>3</sub>), Niobium Pentoxide (Nb<sub>2</sub>O<sub>5</sub>), Strontium Bismuth Tantalate (SBT), Hafnium Oxide (HfO<sub>2</sub>), Hafnium Silicate, Lanthanum Oxide (La<sub>2</sub>O<sub>3</sub>), Yttrium Oxide (Y<sub>2</sub>O<sub>3</sub>), and Zirconium Silicate.

45. (original) A method of forming a capacitor of claim 44, wherein said dielectric layer is formed of a material selected from the group consisting of: Tantalum Oxide, Tantalum Pentoxide (Ta<sub>2</sub>O<sub>5</sub>), Barium Strontium Titanate (BST), Strontium

Bismuth Tantalate (BST), Aluminum Oxide ( $\text{Al}_2\text{O}_3$ ), Zirconium Oxide ( $\text{ZrO}_2$ ) and Hafnium Oxide ( $\text{HfO}_2$ ).

46. (original) A method of forming a capacitor of claim 45, wherein said dielectric layer is Tantalum Oxide and is crystalline or amorphous material.

47. (original) A method of forming a capacitor of claim 46, wherein said amorphous dielectric layer is heated to a temperature above 200 degrees Celsius to change said dielectric layer from an amorphous material to a crystalline material.

48. (original) A method of forming a capacitor of claim 32, wherein said top conducting layer is formed of a material selected from the noble metal group.

49. (original) A method of forming a capacitor of claim 32, wherein said top conducting layer is formed of a non-oxidizing metal permeable to oxygen.

50. (original) A method of forming a capacitor of claim 32, wherein said top conducting layer is formed of a conducting metal oxide.

51. (original) A method of forming a capacitor of claim 32, wherein said top conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), Platinum Iridium (PtIr), Ruthenium, Ruthenium Oxide ( $\text{RuO}_2$ ), Rhodium Oxide ( $\text{RhO}_2$ ), Chromium Oxide ( $\text{CrO}_2$ ), Molybdenum Oxide ( $\text{MoO}_2$ ), Rhemium Oxide ( $\text{ReO}_3$ ), Iridium Oxide ( $\text{IrO}_2$ ), Titanium

Oxides ( $\text{TiO}_1$  or  $\text{TiO}_2$ ), Vanadium Oxides ( $\text{VO}_1$  or  $\text{VO}_2$ ), and Niobium Oxides ( $\text{NbO}_1$  or  $\text{NbO}_2$ ).

52. (original) A method of forming a capacitor of claim 51, wherein said top conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), and Platinum Iridium (PtIr).

53. (original) A method of forming a capacitor of claim 32, wherein said bottom and top conducting layers are formed of a material selected from the group consisting of: Platinum, Platinum Rhodium (PtRh), or Platinum Iridium (PtIr) and said dielectric layer is a layer of Tantalum Oxide.

54. (original) A method of forming a capacitor of claim 32, wherein said bottom and top conducting layers are formed of a material selected from the group consisting of: Platinum, Platinum Rhodium (PtRh), or Platinum Iridium (PtIr) and said dielectric layer is a layer of Barium Strontium Titanate (BST) or Strontium Bismuth Tantalate (SBT).

55. (original) A method of forming a capacitor of claim 32, wherein said top conducting layers are formed of a material selected from the group consisting of: Platinum, Platinum Rhodium (PtRh), or Platinum Iridium (PtIr) and said bottom conducting layer is a layer of Tungsten Nitride ( $\text{WN}_x$ , WN or  $\text{W}_2\text{N}$ ) layer and said dielectric layer is a layer of Aluminum Oxide ( $\text{Al}_2\text{O}_3$ ).

56. (original) A method of forming a capacitor of claim 32, wherein said annealing is performed with an oxidizing gas.

57. (original) A method of forming a capacitor of claim 56, wherein said annealing is performed with a material selected from the group consisting of: Oxygen ( $O_2$ ), Ozone ( $O_3$ ), Nitrous Oxide ( $N_2O$ ), Nitric Oxide ( $NO$ ), and water vapor ( $H_2O$ ).

58. (original) A method of forming a capacitor of claim 57, wherein said annealing is performed with a gas mixture containing at least one element selected from the group consisting: Oxygen ( $O_2$ ), Ozone ( $O_3$ ), Nitrous Oxide ( $N_2O$ ), Nitric Oxide ( $NO$ ), and water vapor ( $H_2O$ ).

59. (original) A method of forming a capacitor of claim 56, wherein said annealing is a plasma enhanced annealing.

60. (original) A method of forming a capacitor of claim 59, wherein said annealing is a remote plasma enhanced annealing.

61. (original) A method of forming a capacitor of claim 56, wherein said annealing is an ultraviolet light enhanced annealing.

62. (original) A method of forming a capacitor of claim 32, wherein said annealing is performed at a temperature between 300 and 800 degrees Celsius.

63. (original) A method of forming a capacitor of claim 62, wherein said annealing is performed at a temperature between 400 and 750 degrees Celsius.

64. (original) A method of forming a capacitor of claim 32, wherein said annealing is performed at a pressure between 1 and 760 torr.

65. (original) A method of forming a capacitor of claim 64, wherein said annealing is performed at a pressure between 2 and 660 torr.

66. (original) A method of forming a capacitor of claim 32, wherein said annealing is performed for between 10 seconds and 60 minutes.

67. (original) A method of forming a capacitor of claim 66, wherein said annealing is performed for between 10 seconds and 30 minutes.

68. (original) A method of forming a capacitor of claim 32, wherein said annealing is performed in the presence of an oxygen as with a gas flow rate between 0.01 and 10 liters per second.

Claims 69-96 (canceled).

97. (New) A method of forming a capacitor in a semiconductor device, said method comprising:

forming a bottom conducting layer, wherein said bottom conducting layer forms a bottom electrode;

forming a dielectric layer over the bottom conducting layer;

forming a top electrode over said dielectric layer, said top electrode comprising at least one top conducting layer; and

annealing said at least one top conducting layer of said top electrode with an oxidizing gas anneal.